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REPORT NO. 94

ON THE DYNAMIC DESIGN OF NON-REGENERATIVE TRANSISTOR CIRCUITS

by

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November 19, 1959
Retyped November 2, 1962

This work was supported in part by the
Atomic Energy Commission and the Office of Naval Research
under Contract AT(11-1)-415

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On the Dynamic Design of Non-Regenerative Transistor Switching Circuits

1. Introduction

In designing a computer, the switching time of a circuit is one of the major considerations. It is directly related to the "economy" of the system. Let W, τ, and c be the total work to be done by a machine (in bits per second), the switching time of a logical element (in seconds per bit), and the cost of a logical element (in dollars), respectively. Then the total cost of the machine, C_T, will be roughly estimated

$$C_T = W^{\tau} c \text{ dollars.}$$

Therefore the cost per unit work to be done by the machine, i.e., the "economy" of the system is

$$C_T/W = {}^{\tau}c. \tag{1}$$

Equation (1) demonstrates the economical aspect of the switching time.

In this report, firstly, the transfer function of a non-regenerative, base-driven transistor circuit is derived by applying the linear equivalent circuit method. The results are experimentally verified. Secondly, the idea of the inverse-gain-bandwidth is introduced as the criterion of the dynamic design. Thirdly, the stability factor is explained. Finally, it is shown that a system constructed by various types of transistor switching circuits is reduced to a long train of unit chains formed by delay units and wave-shapers, and the maximum allowable number of delay units in a unit chain is discussed. The results given here are consistent with the design procedures for transistor switching circuits established in the Digital Computer Laboratory, i.e., the emitter-follower logical circuits associated with restorers and flipflops.

2. Transient Response of Base-Driven Transistor Circuits

2.1 Equivalent circuit of transistor circuits in the active region

Various equivalent circuits were proposed[1,2,3,4] and successfully applied for small signal inputs in the active (linear) region. In reality the operation

of switching circuits is neither in the small signal region nor linear. However, the following reasons guarantee the application of the equivalent circuit method to the switching circuit analysis:

1) transistors are operated in the non-saturating mode,
2) transistor characteristics are fairly linear in the active region,[4]
3) slight nonlinearity may be corrected by taking time averages.

The equivalent circuit method may be applied to any circuit configuration. Only the base-driven circuits are treated in this report because of their wide application in a system.

Figure 1 shows the equivalent circuit and Table 1 gives the parameters.

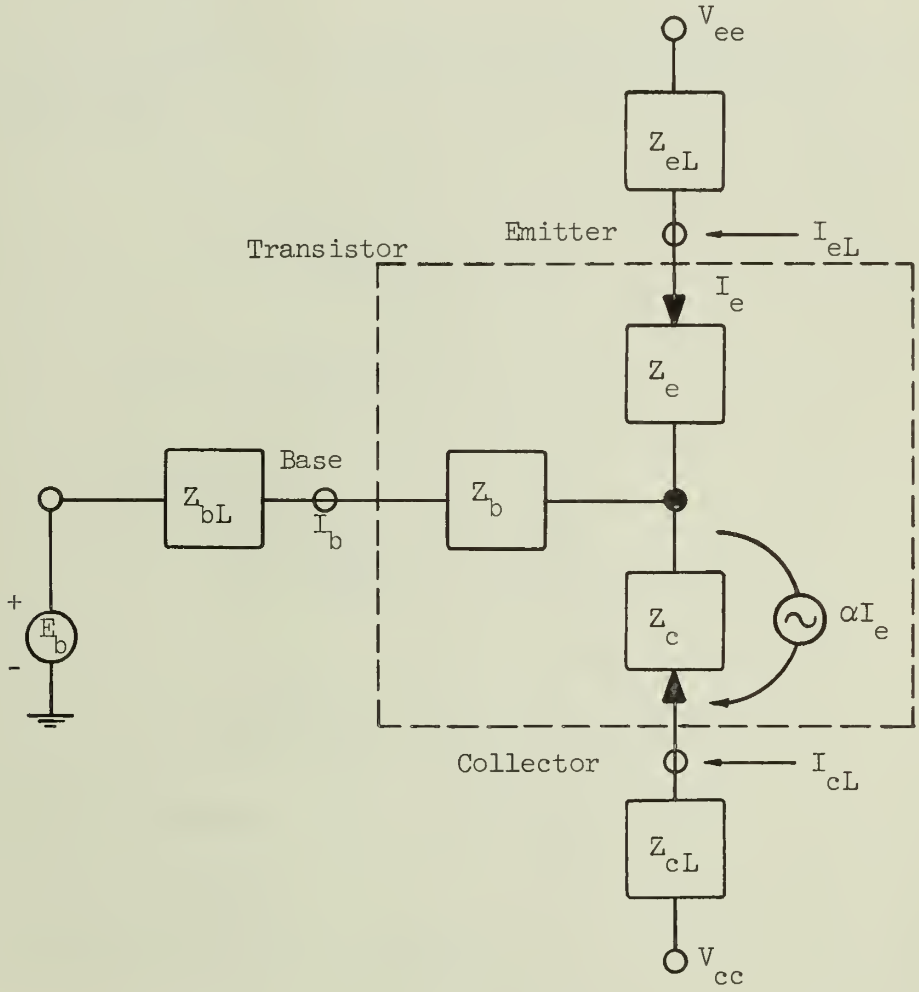


Figure 1: Equivalent Circuit

Table 1

V_{ee} = Emitter supply voltage

V_{cc} = Collector supply voltage

E_b = Base input signal

Z_{eL} = Emitter load

Z_{cL} = Collector load

Z_{bL} = Signal output impedance

I_{eL} = Emitter load current

I = Collector load current

I_e = Transistor emitter current

I_c = Transistor collector current

I_b = Transistor base current

Z_e = Emitter impedance of transistor

Z_c = Collector impedance of transistor

Z_b = Base impedance of transistor

α = Transistor alpha (normal)

α_o = Transistor dc alpha (normal)

In the active region, the transistor parameters will be expressed by Equations (2) through (6):

$$Z_e = \frac{r_e}{1 + sr_eC_{se}} \tag{2}$$

$$Z_c = \frac{r_c}{1 + sr_cC_c} \tag{3}$$

$$Z_b = r_b' \tag{4}$$

$$\alpha = \operatorname{sech}\left\{ \frac{W}{D_m\tau_m} \left(1 + s_m\right) \right\} \tag{5}$$

$$\cong \frac{\alpha_o}{1 + s\tau_\alpha} \tag{6}$$

where r_e = emitter resistance

r_c = collector resistance

r_b' = base spreading ohmic resistance

C_{se} = emitter diffusion capacity $\simeq \dfrac{1}{1.5 r_e \omega_\alpha}$ [3, 10]

C_c = collector depletion layer capacity

ω_α = $1/\tau_\alpha$ = normal alpha cutoff frequency

W = base width

D_m = diffusion constant for minority carriers

τ_m = average lifetime of minority carriers

Equation (5) fits for the case of low level injection and small base width.[5,6,7] Equation (6) is a fairly good approximation of Equation (5) with a correction factor.[8]

Let us assume the loads resistive, then:

$$Z_{et} \equiv Z_{eL} + Z_e , \quad Z_{ct} \equiv Z_{cL} + Z_c , \quad Z_{bt} \equiv Z_{bL} + Z_b$$

and

$$Z_{eL} \equiv R_{eL} , \quad Z_{cL} \equiv R_{cL} , \quad Z_{bL} \equiv R_{bL}$$

$$R_{eL} + r_e \equiv R_{et} , \quad R_{bL} + r'_b \equiv R_{bt} .$$

Then the equivalent circuit shown in Figure 1 leads to the following circuit parameters.

2.1.1 Base input impedance (Z_b) in

$$(Z_b)_{in} = Z_b + Z_{et} \; \frac{1 + \dfrac{Z_{cL}}{Z_c} + \dfrac{\dfrac{Z_{bt}\,Z_{et}}{Z_{ct}}}{Z_{bt} + Z_{et}}}{1 - \alpha + \dfrac{Z_{cL}}{Z_c} + \dfrac{\dfrac{Z_{bt}\,Z_{et}}{Z_c}}{Z_{bt} + Z_{et}}}$$

$$\cong r_b' + Z_{et}\left(1 + \frac{\alpha_o}{1 - \alpha_o + \dfrac{R_{cL} + R_T}{r_c} + s\tau_\alpha\,[1 + \omega_\alpha\,(R_{cL} + R_T)\,C_c]}\right) \tag{7}$$

provided that $\dfrac{R_{cL} + R_T}{r_c} \ll \alpha_o \simeq 1$ (This is assumed hereafter.)

where $R_T = \dfrac{R_{et} R_{ct}}{R_{et} + R_{bt}}$.

2.1.2 Collector current I_c

$$I_c = \frac{\alpha}{1 - \alpha\dfrac{Z_{bt}}{Z_{bt} + Z_{et}} + \dfrac{Z_{cL}}{Z_c} + \dfrac{Z_{bt} Z_{et}}{Z_c(Z_{bt} + Z_{et})}} \quad \frac{E_b - V_{ee} - R_{eL} I_{eL}}{Z_{bt} + Z_{et}}$$

$$\cong \frac{\alpha_o}{1 - \alpha_o\dfrac{R_{bt}}{R_{bt} + R_{et}} + \dfrac{R_{cL} + R_T}{r_c} + s\tau_\alpha[1 + \omega_\alpha(R_{cL} + R_T)C_c]} \quad \frac{E_b - V_{ee} - R_{eL} I_{eL}}{R_{bt} + R_{et}} \tag{8}$$

2.1.3 Emitter current I_e

$$I_e = -\left(1 + \frac{\alpha\dfrac{Z_{bt}}{Z_{bt} + Z_{et}}}{1 - \alpha\dfrac{Z_{bt}}{Z_{bt} + Z_{et}} + \dfrac{Z_{cL}}{Z_c} + \dfrac{Z_{et} Z_{bt}}{Z_c(Z_{bt} + Z_{et})}}\right)\frac{E_b - V_{ee} - R_{eL} I_{eL}}{Z_{bt} + Z_{et}}$$

$$\cong -\left(1 + \frac{\alpha_o\dfrac{R_{bt}}{R_{bt} + R_{et}}}{1 - \alpha_o\dfrac{R_{bt}}{R_{bt} + R_{et}} + \dfrac{R_{cL} + R_T}{r_c} + s\tau_\alpha[1 + \omega_\alpha(R_{eL} + R_T)C_c]}\right) \frac{E_b - V_{ee} - R_{eL} I_{eL}}{R_{bt} + R_{et}} \tag{9}$$

2.1.4 Collector voltage gain A_c

$$A_c = -\frac{\Delta I_e}{\Delta E_b} R_{cL} \cong \frac{-\alpha_o}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c} + s\tau_\alpha[1 + \omega_\alpha(R_{cL} + R_T)C_c]} \cdot \frac{R_{cL}}{R_{bt} + R_{et}} \qquad (10)$$

2.1.5 Emitter voltage gain A_e

$$A_e = -\frac{\Delta I_e}{\Delta E_b} R_{eL} = \left(1 + \frac{\alpha_o \frac{R_{bt}}{R_{bt} + R_{et}}}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c} + s\tau_\alpha[1 + \omega_\alpha(R_{cL} + R_T)C_c]}\right) \cdot \frac{R_{eL}}{R_{bt} + R_{et}} \qquad (11)$$

2.1.6 Collector output impedance $(Z_c)_{out}$

$$(Z_c)_{out} = Z_{cL} \qquad (12)$$

2.1.7 Emitter output impedance $(Z_e)_{out}$

$$(Z_e)_{out} = Z_{eL}(1 - A_e) \qquad (13)$$

2.2 Solutions in the time domain

2.2.1 Collector output voltage V_c

Collector output voltage for voltage amplifying circuits will be obtained by equation (10) for unit step function.

$$V_c = -\Delta I_c R_{cL} = -|A_c|(1 - e^{-t/T_c})E_b \qquad (14)$$

where

$$|A_c| = \frac{\alpha_o}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c}} \quad \frac{R_{cL}}{R_{bt} + R_{et}} \tag{15}$$

$$T_c = \frac{\tau_\alpha[1 + \omega_\alpha(R_{cL} + R_T)C_c]}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c}} \tag{16}$$

$$\cong (1 + \omega_\alpha R_{cL} C_c) \frac{\tau_\alpha}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}}} \tag{17}$$

provided that $R_{eL} = 0$.

2.2.2 Emitter output voltage V_e

$$V_e = -R_{eL}\Delta I_e = \frac{R_{eL}E_b}{R_{bt} + R_{et}} + \frac{\alpha_o}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c}} \quad \frac{R_T E_b}{R_{bt} + R_{et}}(1 - e^{-t/T_c})$$

$$= (|A_e| - |A_e'|\, e^{-t/T_c})E_b \tag{18}$$

where

$$|A_e| = \frac{R_{eL}}{R_{bt} + R_{et}} + \frac{\alpha_o}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c}} \quad \frac{R_T}{R_{bt} + R_{et}} \tag{19}$$

$$|A_e'| = \frac{\alpha_o}{1 - \alpha_o \frac{R_{bt}}{R_{bt} + R_{et}} + \frac{R_{cL} + R_T}{r_c}} \quad \frac{R_T}{R_{bt} + R_{et}} \tag{20}$$

If the time constant is defined by the time it takes the voltage to reach (1 - 1/e) of its final value, then the time constant of the emitter output voltage is

$$T_e = T_c \left[1 - \ln \frac{|A_e|}{|A'_e|}\right] < T_c \tag{21}$$

or

$$\simeq \frac{R_{eL}}{R_T} \; \frac{[1 + \omega_\alpha (R_{cL} + R_T) c_c]\, \tau_\alpha}{\alpha_o}$$

$$= \left(\frac{R_{eL}}{R_T} + \omega_\alpha R_{eL} C_c \right) \frac{\tau_\alpha}{\alpha_o} \tag{22}$$

provided that $R_{cL} = 0$.

2.3 Inverse gain-band-width

A first glance at equations (15)-(22) will give us the following remarkable evidence. "The time constant generally increases as the gain increases." This statement is true both for the same circuit configuration with different parameters and for the different circuit configuration. Take a collector follower as an example. Suppose two transistors whose alphas are α_{o1} and α_{o2} respectively are interchanged in the same socket.

$$|A_{c1}| \simeq \frac{\alpha_{o1}}{1 - \alpha_{o1}} \; \frac{R_{cL}}{R_{bt}}$$

$$|A_{c2}| \simeq \frac{\alpha_{o2}}{1 - \alpha_{o2}} \; \frac{R_{cL}}{R_{bt}}$$

$$T_{c1} \simeq \frac{1 + \omega_{\alpha 1} R_{cL} c_{c1}}{1 - \alpha_{o1}} \; \tau_{\alpha 1}$$

$$T_{c2} \simeq \frac{1 + \omega_{\alpha 2} R_{cL} c_{c1}}{1 - \alpha_{o2}} \; \tau_{\alpha 2}$$

The variation of $1 - \alpha_o$ may be as much as 400%. Consequently, $|A_{c1}|/|A_{c2}|$ and T_{c1}/T_{c2} varies from 25% to 400%. However the variation of $T_c/|A_c|$ is far less than that of $1 - \alpha_o$. Let us compare a collector follower with an emitter follower:

$$k_c = \frac{T_c}{|A_c|} \simeq \frac{R_{bt}}{R_{cL}} \frac{(1 + \omega_\alpha R_{cL} C_c) \tau_\alpha}{\alpha_o}$$

$$k_e = \frac{T_e}{|A_e|} \simeq \frac{R_{eL}}{R_T} \frac{(1 + \omega_\alpha R_T C_c) \tau_\alpha}{\alpha_o} .$$

Estimating with possible magnitudes of parameters, it will be easily found that k_c has the same order of magnitude as k_e.

It is a well-known fact that a high gain-band-width product is the condition for the high fidelity waveform propagation. Since we are interested in the switching time, the concept of "inverse gain-band-width" will be introduced at this point. It is defined by equation (23).

$$k = \frac{T}{|A|} \tag{23}$$

$$k_c = \frac{R_{bt} + R_{et}}{R_{cL}} \frac{[1 + \omega_\alpha (R_{cL} + R_T) C_c]}{\alpha_o} \tau_\alpha \tag{23.a}$$

$$k_e = \frac{R_{eL}}{R_T} \frac{[1 + \omega_\alpha (R_{eL} + R_T) C_c]}{\alpha_o} \tau_\alpha \tag{23.b}$$

Yokelson et.al. defined the inherent inverse gain-band-width of transistors as $1/\omega_\alpha \alpha_o = \tau_\alpha/\alpha_o$.[9] However their definition is not sufficient because the collector capacitor has a dominent effect on the switching time as shown later. The circuit-wise inverse gain-band-width has a form $(1 + \omega_\alpha R_L C_c)\ \tau_\alpha/\alpha_o$. Stray capacitances take up the same position as C_c in the equation of k. Therefore, the term $\omega_\alpha R_L C_c$ will become an important factor as ω_α increases.

The significance of the inverse gain-band-width will be thoroughly discussed in sections 4 and 5.

2.4 Non-linearity

2.4.1 Methods of compensation for non-linearity

It was concluded in the former section that the transfer function of transistor switching circuits may be represented by equation (24) and shown by Figure 2.

$$G(s) = \frac{A}{1 + sT} \tag{24}$$

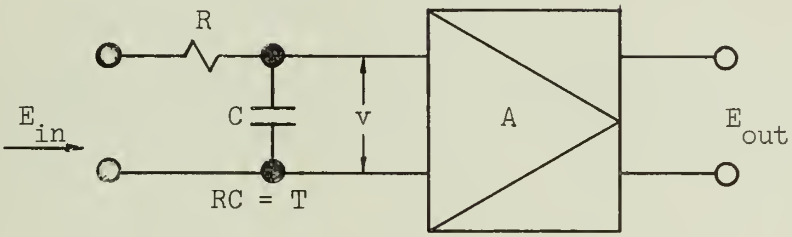


Figure 2: Schematic Equivalent Circuit

However, A and T are by no means constants because of the non-linearity of actual circuits. They are functions of v. The voltage differential equation is, therefore, modified as follows:

$$T(v) \frac{dv}{dt} + v = E_{in} \tag{25.a}$$

$$E_{out} = v \cdot A(v) \quad . \tag{25.b}$$

The time average of the first term of equation (25.a) is

$$\frac{1}{t_2 - t_1} \int_{t_1}^{t_2} T(v) \frac{dv}{dt} \cdot dt = \left[\frac{1}{v_2 - v_1} \int_{v_1}^{v_2} T(v) dv \right] \frac{v_2 - v_1}{t_2 - t_1}$$

$$\Longrightarrow \left[\frac{1}{v_2 - v_1} \int_{v_1}^{v_2} T(v) dv \right] \cdot \frac{dv}{dt} = \hat{T} \frac{dv}{dt} \quad . \tag{26}$$

The discrepancy caused by non-linearity will be remarkably improved by using $\hat{T}$ instead of a time constant calculated by linear assumptions. v_1 and v_2 denote the initial and terminal operating points of the associated transistor. Since the direct calculation of $\hat{T}$ by the equation (26) is very laborious, the parameters related to time constants will be separately calculated by the same principle and inserted into the linear equations mentioned in the former section.

A(v), however, should not be the time average because steady state solutions must agree with the steady state values of the transient solutions. Therefore

$$\hat{A} = A(v_2) - A(v_1) \tag{27}$$

i.e., $\hat{A}$ is the difference of the initial and the terminal points. There could be two correction forms for the same parameter. $\hat{A}$ will be estimated exactly by dc-circuit analysis.

2.4.2 Emitter resistance r_e

The main non-linearity is attributed to the emitter resistance r_e and the transistor alpha α. The emitter current I_E in the active region is expressed in equation (28) obtained from a diode junction analogy.[4]

$$I_E = I'_E(e^{V/V_o} - 1) + I''_E \tag{28}$$

where V is the emitter junction voltage.

The incremental emitter resistance r_e is

$$r_e = \frac{V_o}{I_E + I'_E} \tag{29}$$

$$\therefore \quad \hat{r}_e = \frac{1}{I_{E_2} - I_{E_1}} \int_{I_{E_1}}^{I_{E_2}} r_e dI_E = \frac{V_o}{I_{E_2} - I_{E_1}} \ln\left(\frac{I_{E_2} + I'_E}{I_{E_1} + I'_E}\right) \tag{30}$$

At room temperature, $V_o = 0.026$ volt. I'_E may be determined experimentally. The r_e remains unchanged for the same output $\Delta I_E = I_{E_2} - I_{E_1}$ if $I_{E_2}/I_{E_1} \cong 1$. Incidentally, I'_E ranges from 2 to 10 μa usually.

2.4.3 Alpha α_o

The alpha α_o will change as shown in Figure 3. "The A-B portion results from the building up in the base region of a field which assists the transit of the minority carrier".[6] "The B-C portion is owing to the decrease in injection efficiency."[6] After reaching saturation point C, $\hat{\alpha}_o$ decreases steeply. This curve will be measured and $\hat{\alpha}_o$ will be obtained from it.

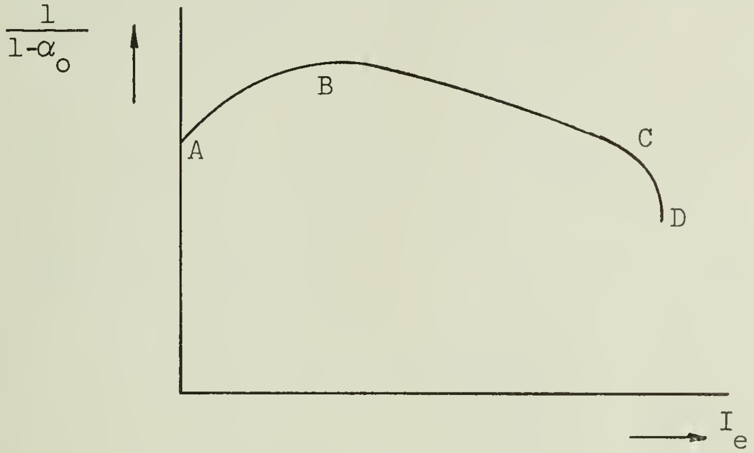


Figure 3: Normal Alpha and Emitter Current

2.4.4 Collector capacity C_c and cutoff frequency ω_α [10]

C_c decreases as the collector voltage negatively increases and as the emitter current decreases. ω_α remains rather unchanged. However, the variation of C_c and ω_α are less significant than that of r_e and α. Therefore it may be neglected for some cases.

3. Experimental Verification

Because of the difficulties in measuring C_c, r_e, r_b', etc., the equations listed in the preceding section were not verified directly. They were verified indirectly by checking the nature of the observed data and by comparing the estimated parameters with their measured values.

The emitter follower's time constant is too fast to be measured with the available equipment. The measurement was accomplished for the collector follower configuration only.

The time constant was defined as the time in which the output voltage reaches (1 - 1/e) of its steady value and measured by comparing the waveform of the circuit with the waveform of the trivial R-C circuits whose time constant is a known value, i.e., RC.

3.1 Linear operation

In order to eliminate every possible non-linearity, the initial point was chosen such that

$E_{in} = 0,\qquad I_{c1} = -4\ \text{ma},\qquad V_{c1} = -10\text{V},$

$R_{eL} = 100\ \Omega\qquad (R_{bL})_{min} = 500\Omega$

$E_{out} = V_{c2} - V_{c1},\qquad |A_c| = \frac{E_{out}}{E_{in}}$

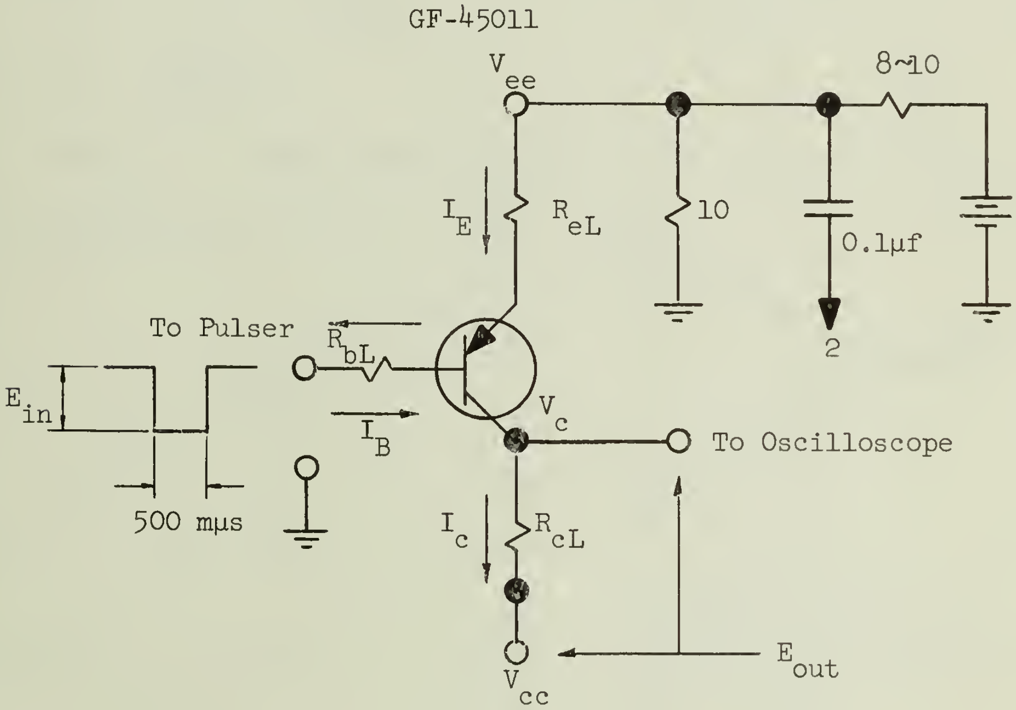
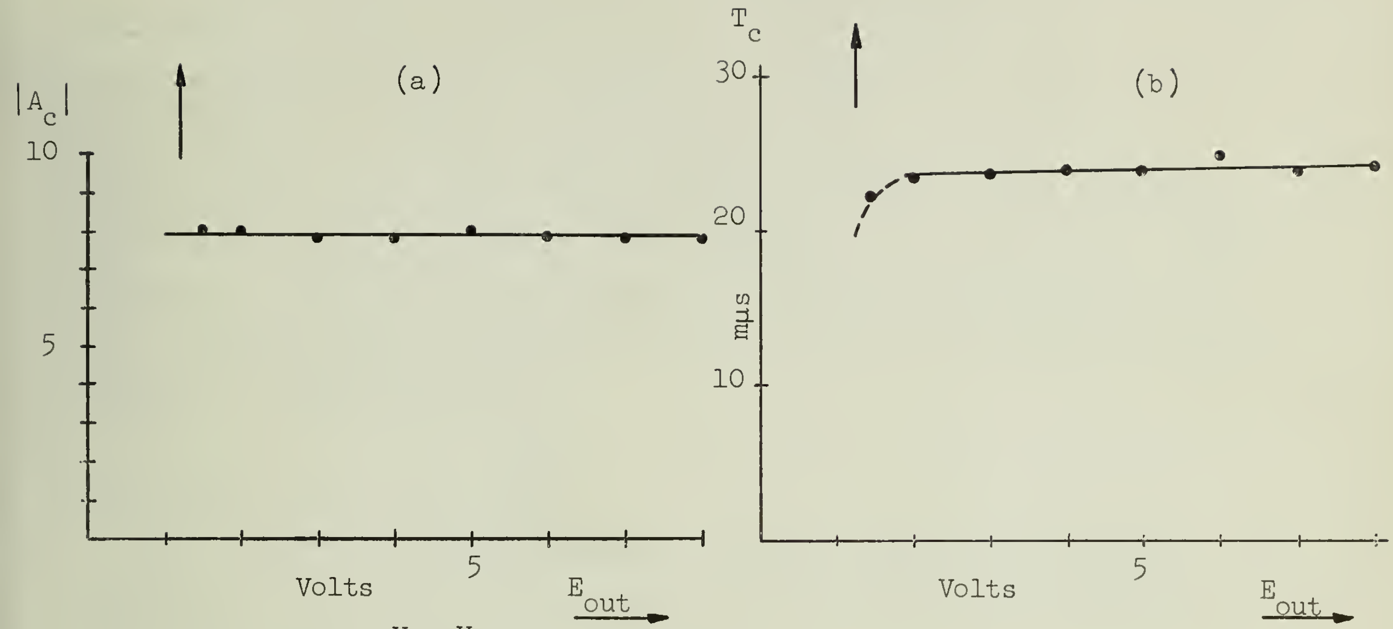


Figure 4: Measuring Circuit

A number of measurements were made, but only a few of them will be shown, for the rest are more or less alike.



$$\text{Gain } |A_c| = \left|\frac{V_{c2}-V_{c1}}{E_{in}}\right|$$

Figure 5: Linear Operation ($R_{cL} = 1000\Omega$, $R_{bL} = 1000\Omega$)

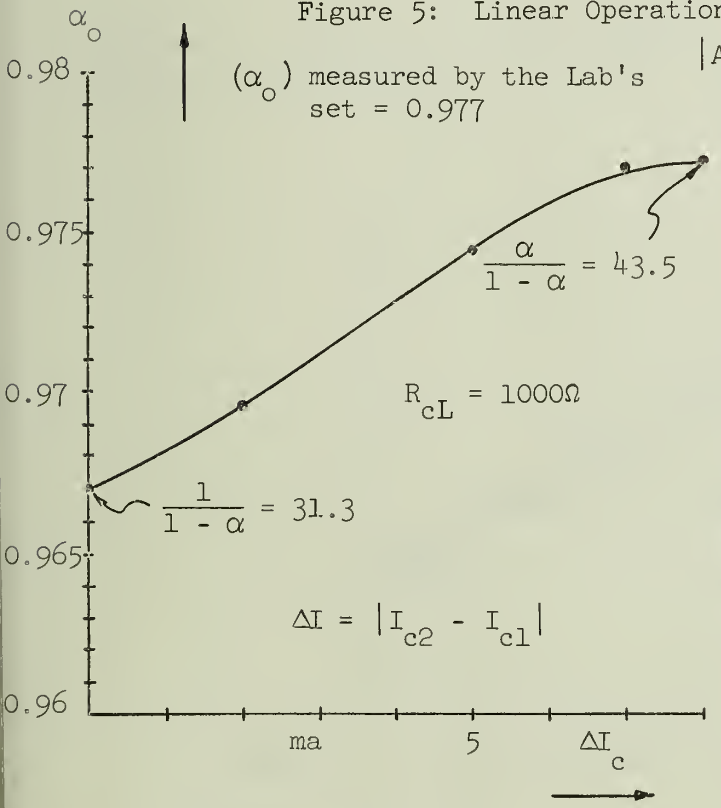


Figure 6: DC Alpha

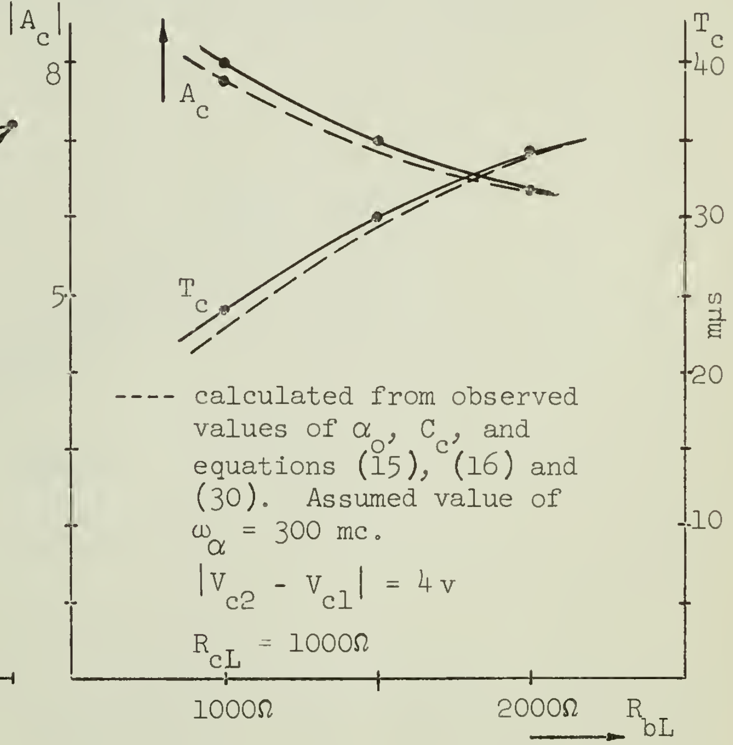


Figure 7: $|A_c|$ and T_c vs. R_{bL}

3.1.1 Linearity in the "linear mode"

Figures 5(a) and (b) show the linearity in the so-called linear mode. (This is not the case for non-linear operation.) The alpha is not so linear. About 30% change in $\frac{1 - \alpha_o}{\alpha_o}$ was observed in the range of 0 to 8 ma of I_c as shown in Figure 6. Figure 7 shows the observed $|A_c|$ and $|T_c|$ vs. R_{bL} characteristics which closely agree with the calculated curves from the estimated c_c, α_o, and ω_α values, using equations (15), (16) and (30). The estimate of c_c and ω_α will be discussed in the following subsection. It may be recognized that the equations (15) and (16) are accurate theoretical formulae for linear operation.

3.1.2 Inverse gain-band-width

Gain $|A_c|$ and time constant T_c are not convenient to analyze. As may be predicted in the equation (23.a), the inverse gain-band-width k_c is linear with respect to R_{bL}, R_{eL}, and $1/R_{cL}$.

The theoretical k_c vs. R_{bL} characteristics is shown in Figure 8. The slope $m = dk_c/dR_{bL}$ and the increment n of the (k_c) axis are very useful indices, especially m.

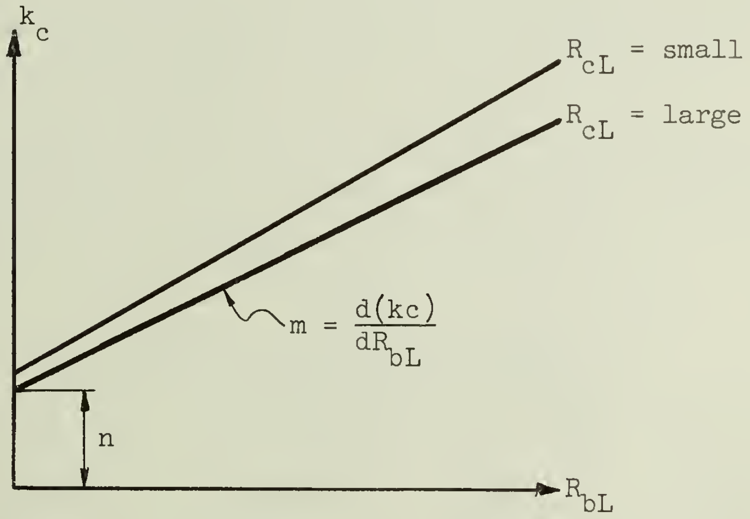


Figure 8: Inverse Gain-Band-Width vs. Signal Output Impedance

From equation (23.a),

$$m = \frac{1}{\alpha_o} \left[\frac{\tau_\alpha}{R_{cL}} + \left(1 + \frac{R_T}{R_{cL}}\right) C_c \right] \tag{31}$$

$$n = (r_b' + R_T)\, m \tag{32}$$

The slope is steeper for smaller R_{cL} than for larger R_{cL}. The asymptotic value of m, corresponding to $R_{cL} = \infty$, will give C_c/α_o.

$$\frac{dm}{d(\frac{1}{R_{cL}})} = \frac{\tau_\alpha}{\alpha_o} + R_T C_c . \quad \text{If } R_T C_c << \frac{\tau'_\alpha}{\alpha_o} \text{, then}$$

$$\frac{dm}{d(\frac{1}{R_{cL}})} = \frac{\tau_\alpha}{\alpha_o} .$$

By this relation we can estimate the cutoff frequency ω_α. The measuring accuracy of n is directly related to that of the time constant. Therefore n was not analyzed, but it agrees with the measured results of m within an order of magnitude. Notice that m is the relative quantity so that it is not as closely related to the measuring accuracy as n is.

Figure 9(a), (b), (c), and (d) is a set of curves of k_c for 2 groups of transistors, i.e., one is large α_o and the other small. The estimated values from Figure 9 of C_c and ω_α are tabulated below.

Table 2

Estimated Values of C_c and ω_α

	$\alpha_o = 0.958$	$\alpha_o = 0.960$	$\alpha_o = 0.986$	$\alpha_o = 0.986$
C_c	2.6 μμf	2.6 μμf	2.5 μμf	1.8 μμf
ω_α	620 mc	650 mc	410 mc	750 mc

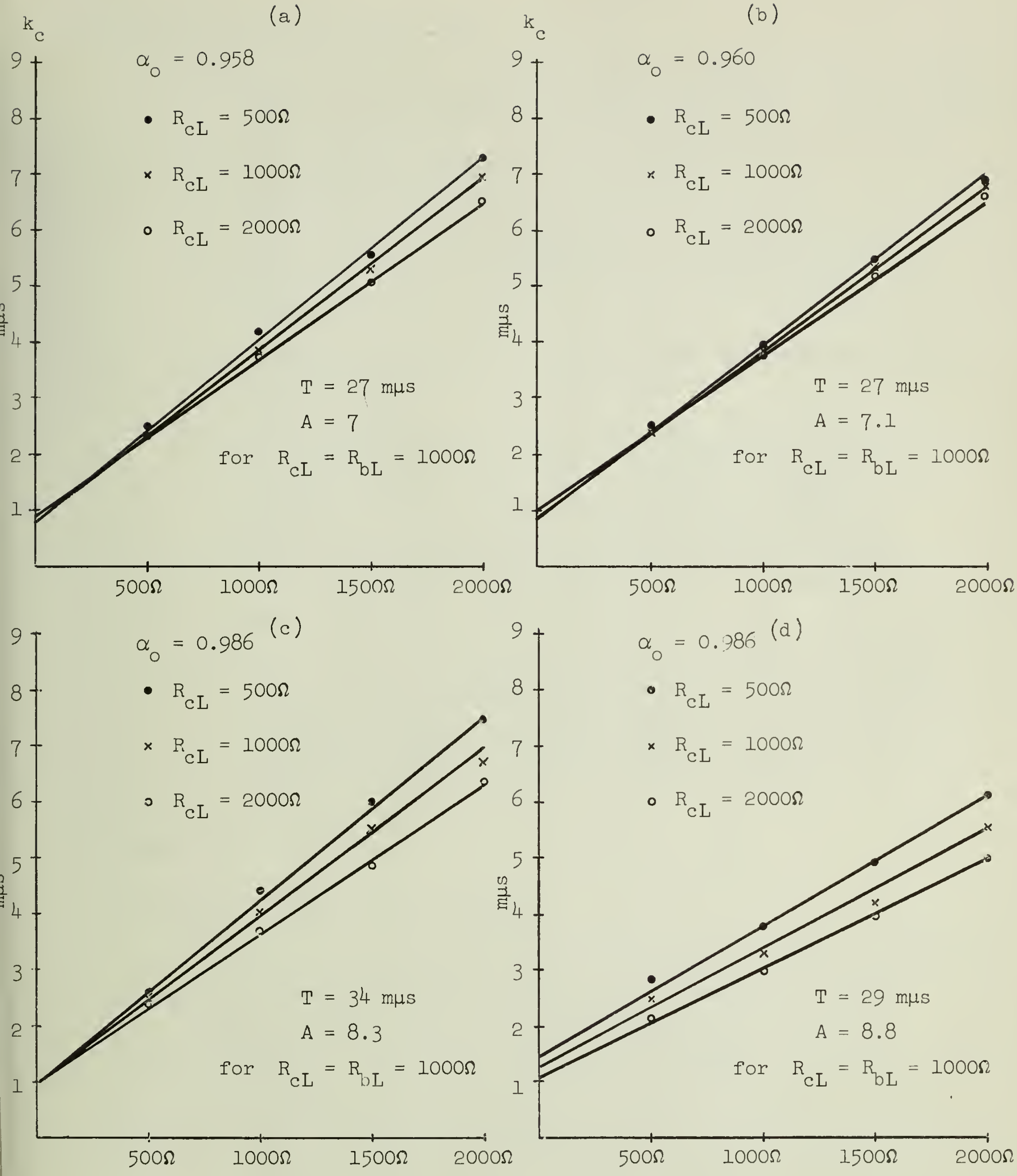


Figure 9: k_c vs. R_{bL} TR = GF45011

The following remarks should be made:

(i) The relation between inverse gain band width and signal output impedance is satisfactorily linear as indicated in equation (23).

(ii) The estimated values of collector capacity and alpha cutoff frequency are reasonable.

(iii) The time constant associated with the collector capacity is greater than that associated with the cutoff frequency for a voltage amplifier.

(iv) The magnitude of the collector capacity seems to have less correlation with alpha.

(v) The minimum obtainable inverse gain-band-width of GF45011 transistors may be about 1 mµs. However, the signal output impedance rapidly increases the inverse gain-band-width. Therefore the signal output impedance should be kept as small as possible. The emitter follower configuration is highly preferable.

(vi) $(1 - \alpha_o)$, i.e., the gain, is not as important factor to the transient speed as might be expected as long as the speed of one logical stage is concerned. However, it becomes very important when the propagation speed of a system matters.

3.2 Non-linear operation

3.2.1 Effect of signal output impedance

As long as the initial operating point and the terminal operating point are kept unchanged, the time average of the transistor parameters (such as shown by equation (26)) and the difference of the transistor parameters (defined by equation (27)) also remain unchanged. Therefore the linear relation between the inverse gain band-width and the signal output impedance may still be preserved, in this case. Let us designate the time average by $\wedge$ and the difference by - ; then the inverse gain-band-width for this case will be described as follows:

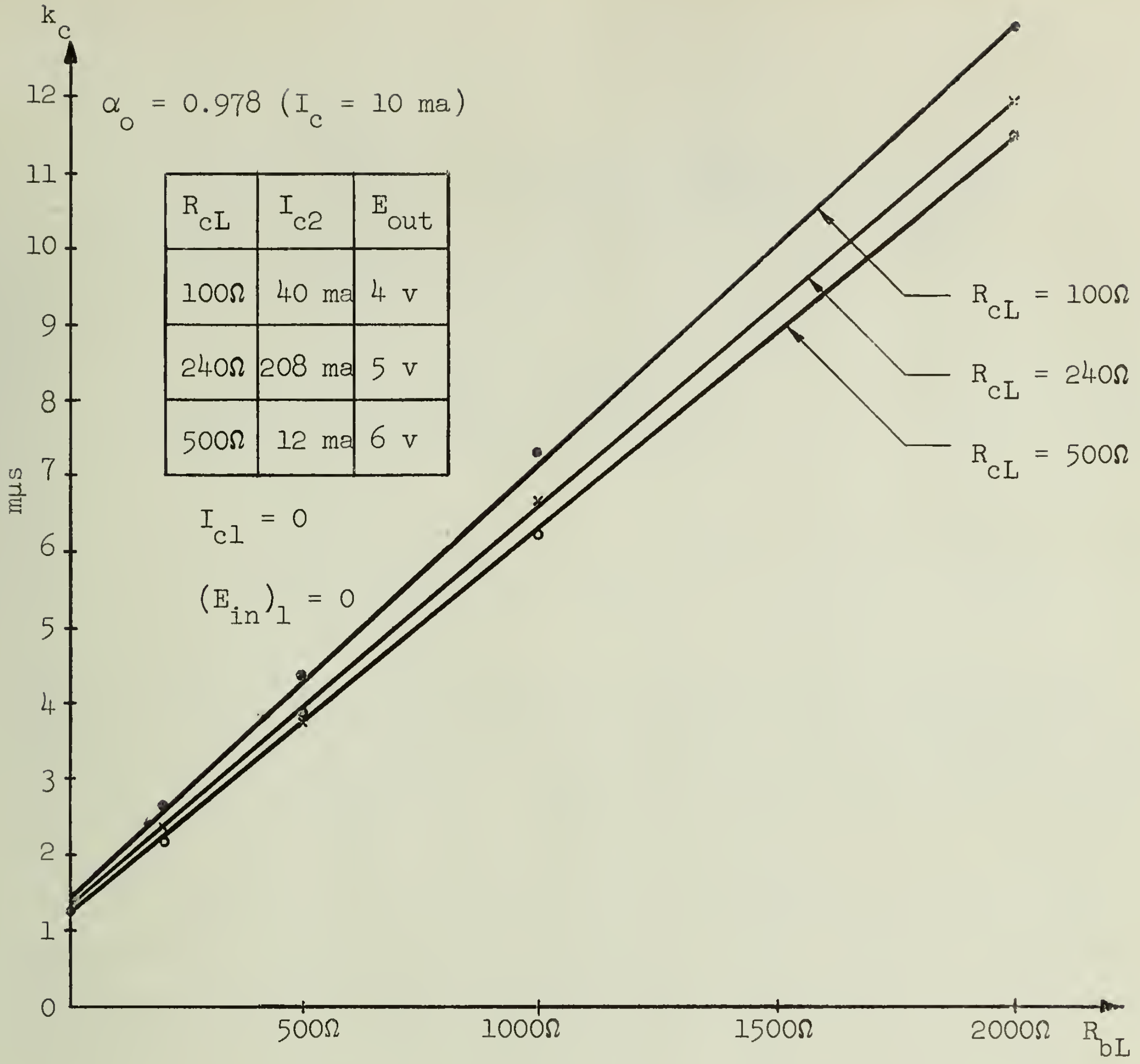


Figure 10: k_c vs. R_{bL} in Non-linear Region

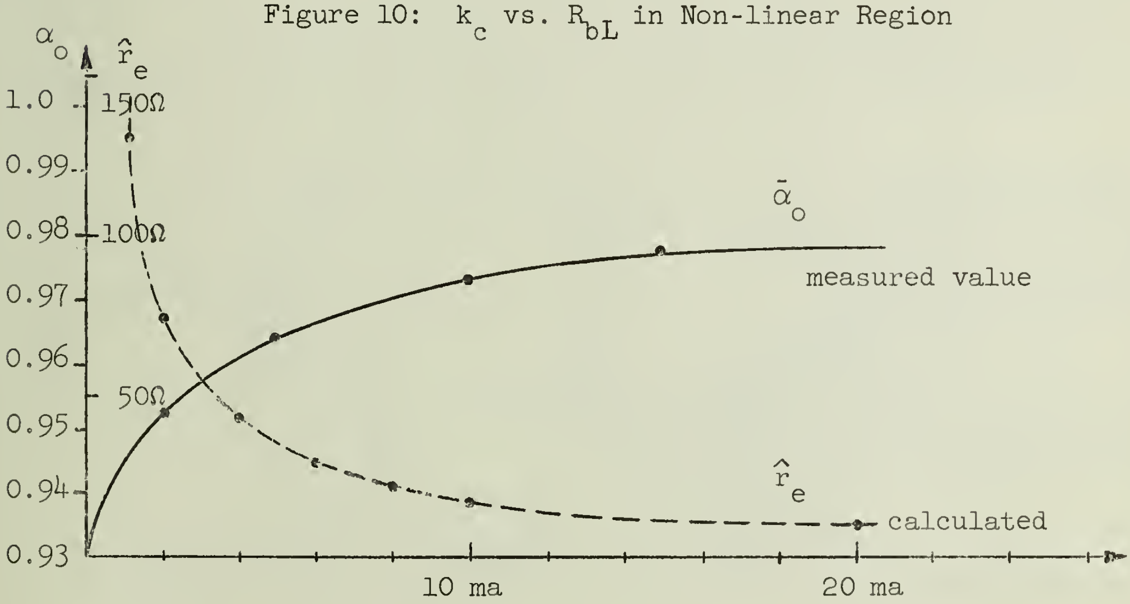


Figure 11: $\bar{\alpha}_o$, $\hat{r}_e$ vs. I_{c2} ($I_{c1} = 0$)

$$k_c \cong \frac{1 - \bar{\alpha}_o \dfrac{R_{bt}}{R_{bt} + \bar{R}_{et}}}{1 - \hat{\alpha}_o \dfrac{R_{bt}}{R_{bt} + \hat{R}_{et}}} \quad \frac{[1 + \omega_\alpha (R_{cL} + \hat{R}_T)\hat{C}_c]\, \tau_\alpha}{\bar{\alpha}_o} \quad \frac{R_{bt} + \bar{R}_{et}}{R_{ct}}$$

$$\cong \frac{R_{bt} + \bar{R}_{et}}{R_{ct}} \quad \frac{[1 + \omega_\alpha (R_{cL} + \hat{R}_T)\hat{C}_c]}{\bar{\alpha}_o}\, \tau_\alpha \qquad (33)$$

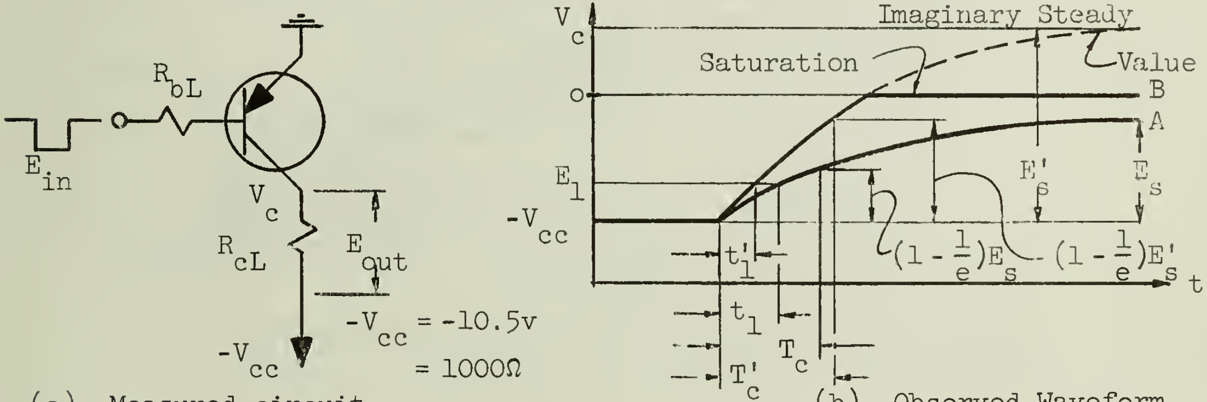
$$\because \quad \bar{\alpha}_o = \hat{\alpha}_o, \ \hat{R}_{et} \ll R_{bt} \quad .$$

Figure 10 shows that k_c varies linearly with R_{bL} even in the non-linear operation region in which $\bar{\alpha}_o$ and $\hat{r}_e$ (for example) reveal considerable non-linearity as shown in Figure 11. Therefore, it seems permissible to neglect the effect of R_{bL} on the non-linear characteristics.

From Figure 10, the value of C_c is estimated at 4.8 μμf. It seems that when transistors turn from the off state to the on state, the effective collector capacity is larger than its steady state value. This may be deduced from the initial build-up of a collector barrier layer.

Because of this effect, the inverse gain-band-width in the non-linear case is about twice as large as that of the linear operation.

3.2.2 Inverse gain-band-width and operation range



(a) Measured circuit (b) Observed Waveform

Figure 12: Measured Circuit and Observed Waveform

As E_{in} increases, the steady state value of the output voltage approaches the saturation region. Then there is no way to define the time constant. However, if one is allowed to set up the imaginary steady state value E'_s as shown in Figure 12(b), then we could define the time constant T'_c and the inverse gain-band-width $k'_c = T'_c/A'_e = T'_c E'_{in}/E'_s$. In practical application, the operation time we are concerned with, t_1, is the time in which the output reaches the pre-specified reference voltage E_r. Even when E_s extends into the saturation region, t_1 is smaller for the larger input swing, though the efficiency falls off.

Figure 13 shows the A_c and T_c vs. E_{out}. Figure 14 shows k_c vs. E_{out} with R_{cL} as a parameter. The imaginary portion (gained by extrapolation) will be distinguished by a dotted line. Figure 15 indicates that there is an optimum value of R_{cL} appropriate to the required output voltage. The behavior shown in Figures 13, 14 and 15 may be explained by the non-linearity of α_o (Figure 3) and $\hat{r}_e$ (equation (30)). It may be noticed that the curve k_c vs. R_{cL} becomes steeper for smaller values of R_{cL} than the appropriate optimum value. It seems to be safer to use a slightly higher value of R_{cL} than the optimum, compromising the collector load current I_{cL}.

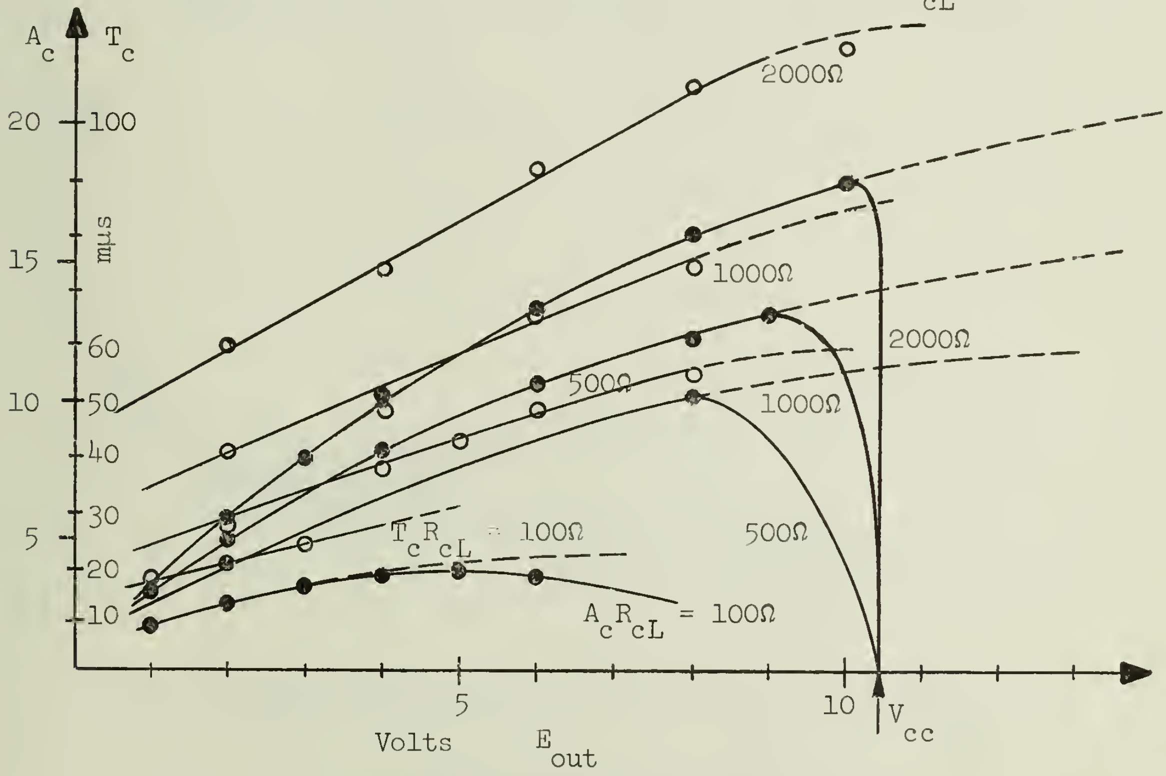


Figure 13: A_c and T_c vs. E_{out}

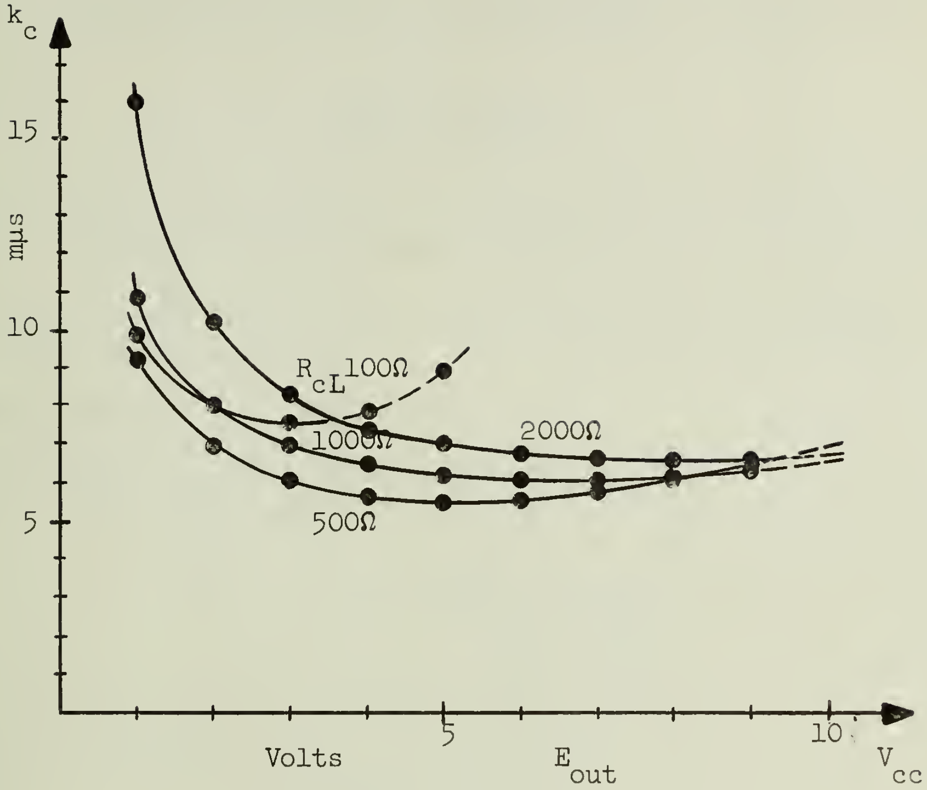
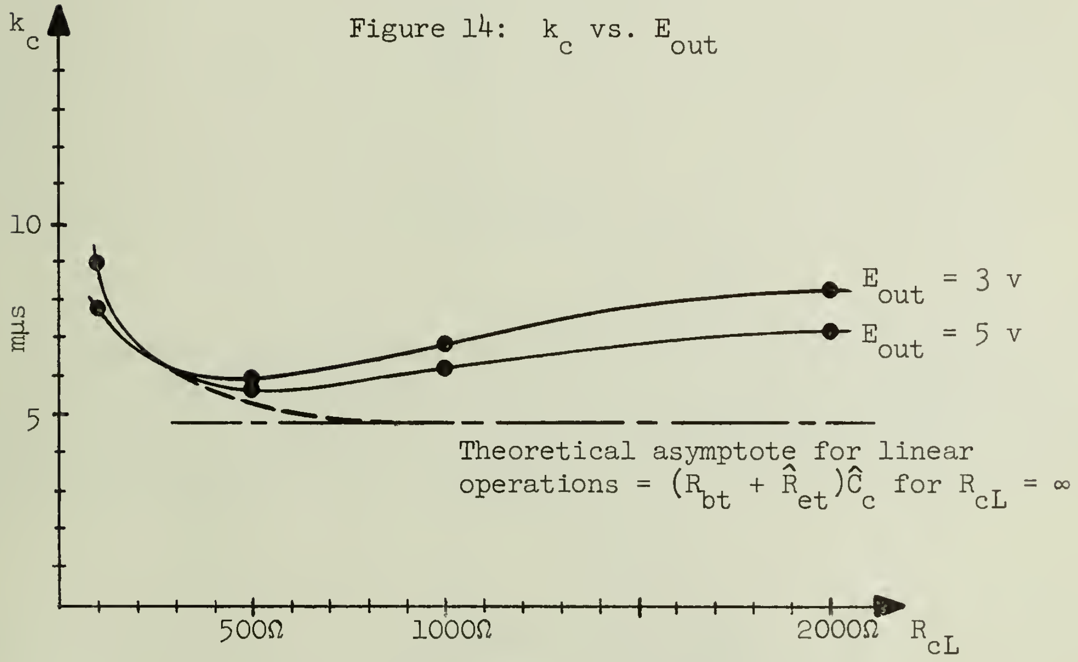


Figure 14: k_c vs. E_{out}



Theoretical asymptote for linear operations = $(R_{bt} + \hat{R}_{et})\hat{C}_c$ for $R_{cL} = \infty$

Figure 15: k_c vs. R_{cL}

4. Switching Time of Non-Regenerative Transistor Circuits

Thus far, it was discussed and experimentally verified that

(i) The transfer function of the non-regenerative transistor switching circuit may be formulated in equation (24):

$$G(s) = \frac{A}{1 + sT}$$

(ii) and that the inverse gain-band-width (k) defined by T/A remains unchanged between transistors and circuit configurations.

Now we shall include G(s) in our switching time analysis.

4.1 Correction factor

The time to reach the reference voltage E_r is

$$t_1 = T \ln \left(\frac{1}{1 - \frac{E_r}{E_s}} \right) .$$

Let us denote

$$\frac{E_r}{E_s} = \frac{1}{F} .$$

Then

$$t_1 = T \ln \left(\frac{1}{1 - \frac{1}{F}} \right) . \qquad (34)$$

Equation (34) has been based upon the approximate equation (6) of α. W. W. Gartner calculated the more exact but complicated form(5).[8] According to his calculation, the more exact time t_1' has a simple relation (35) to t_1, though he did not mention this.

$$t_1' = (F)^{\rho}(t_1) \qquad (35)$$

where $\rho = 0.5$ for common base circuit

$\rho = 0.18 \sim 0.2$ for common emitter circuit

$\rho \cong 0$ for common collector circuit

and is valid for $1 < F < 10$.

If F is a fixed value, F^{ρ} = constant. Therefore we shall consider t_1 for simplicity. The more extended form of α was studied. Unfortunately, however, if is too complicated to use in analyzing the transient behavior of transistor switching circuits.

4.2 Response of G(s) to a constant slope input

The input waveform shown in Figure 16 may be considered as a simplified waveform of dc-logical circuits.

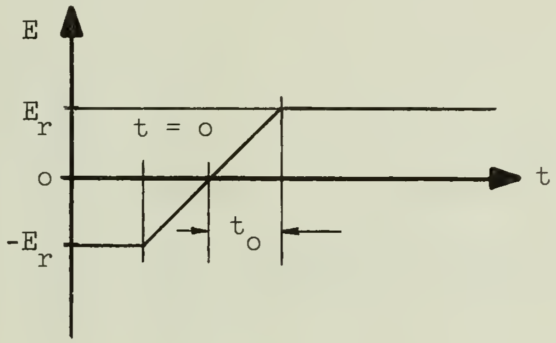


Figure 16: Constant Slope Input

4.2.1 $|A| < 1$, $T < t_o$

$$E_{out}(t) = \mathcal{L}^{-1}\left[\frac{A}{1 + sT}\,\frac{E_r}{s^2 t_o}\left(1 - c^{-2t_o s}\right)\right] - E_r$$

$$\cong \frac{AE_rT}{t_o}\left[\left(\frac{t}{T} - 1\right)\left(\frac{t - 2t_o}{T} - 1\right) u(t - 2t_o)\right] - E_r \qquad (36)$$

Neglecting higher order terms, the output waveform may be of the same transit time $2t_o$, of the damped height $2AE_r$, and of the time lag T.

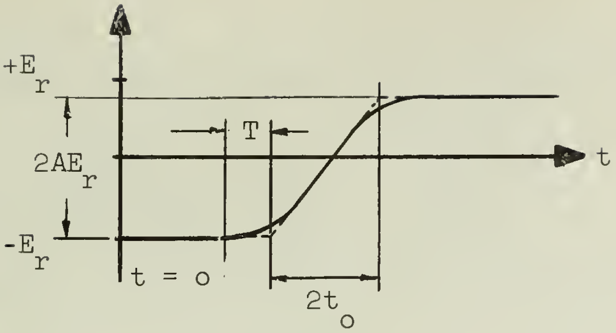


Figure 17: E_{out} for $|A| < 1$, $T < t_o$

4.2.2 $|A| > 1$, $T > t_o$

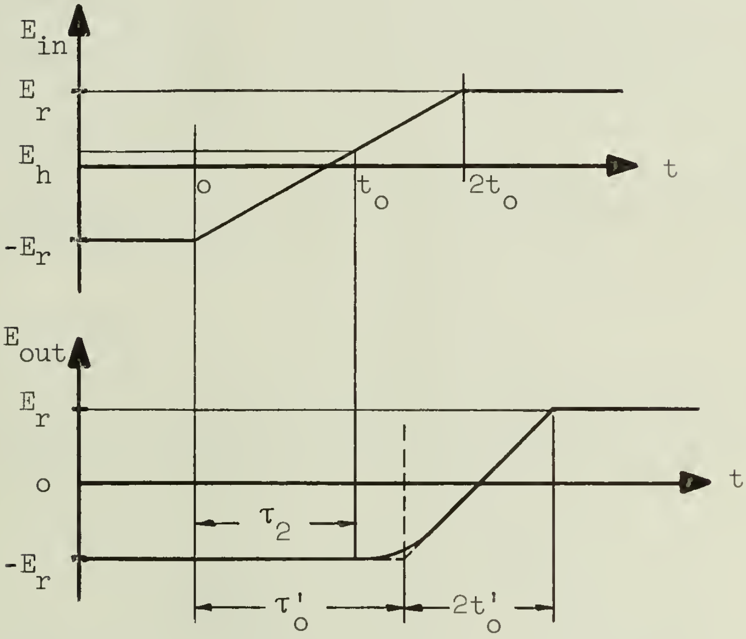


Figure 18: E_{out} and E_{in} for $|A| > 1$, $T > t_o$

The output voltage stays the same until the input voltage reaches the threshold point E_h of the circuit. When the output voltage reaches the reference voltage E_r (or $-E_r$), the output voltage will be clamped to the reference point.

$$E_{out} = \mathcal{L}^{-1}\left[\frac{A}{1+sT}\,\frac{E_r}{s^2 t_o}\left(e^{-\tau_2 s} - e^{-2t_o s}\right)\right] - E_r$$

$$\cong \frac{AE_r}{2T}\left[\left(4 - 2\,\frac{\tau_2}{t_o}\right)t - \left(4 - \left(\frac{\tau_2}{t_o}\right)^2\right)t_o\right]u(t - \tau'_0) - E_r \qquad (36)$$

for $E_{out} < E_r$ where $$\tau'_o = \left(\frac{3}{2} + \frac{1}{2}\,\frac{E_h}{E_r}\right) t_o \qquad (37.a)$$

The transit time t'_o is given by the following equation:

$$t'_o = \frac{(E_r)T}{A(E_r - E_h)} \cong \frac{T}{A} \left(1 + \frac{E_h}{E_r}\right) \quad . \tag{37.b}$$

Assuming $E_h = 0$, and using the inverse gain-band-width $k = T/A$,

$$\tau'_o = \frac{3}{2} t_o \tag{38.a}$$

$$t'_o = k \tag{38.b}$$

The above things will be restated below.

Neglecting higher order terms, the output waveform may be:

of transit time 2k, which doesn't depend on the transit time of the input wave,

of nominal height E_r,

and of time lag $3/4(2t_o)$, i.e., three quarters of the transit time of the input wave.

4.2.3 Regenerative circuit

In order to show the generality of the argument in the following section, the regenerative circuit will be briefly discussed here.

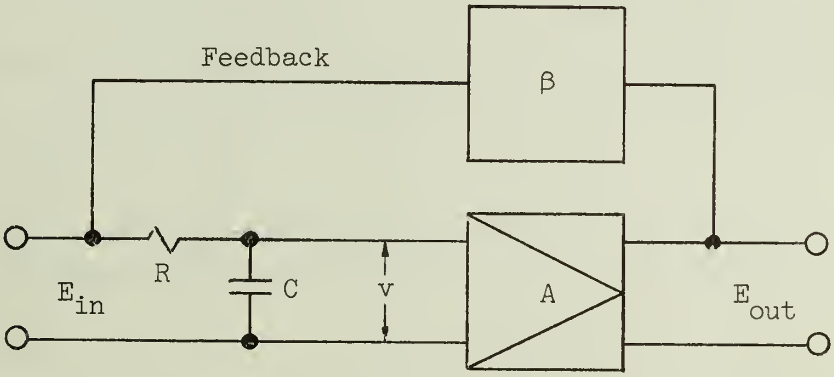


Figure 19: Regenerative Circuit

Figure 19 is a schematic diagram of regenerative circuits. Solving E_{out} with the initial condition $(v)_{t=o} = 0$ and $(\frac{dv}{dt})_{t=0} = I$, E_{out} will be given in form (39)

$$E_{out} = AIT(e^{t/T} - 1) \tag{39}$$

where

$$T = \frac{RC}{\beta A - 1} \quad . \tag{40}$$

Since the circuit is regenerative $\beta A - 1 > 0$, we have a negative time constant.

Since any regenerative circuit uses an amplifier, the gain of which is greater than unity, then the time constant T given by equation (40) may be greater than the time t concerned. If $t/T < 1$ is assumed,

$$E_{out} = AIT\ (1 + \frac{t}{T}\ .\ \dots -1) \cong AIT\ \frac{t}{T}$$

while

$$E_{out} = AE_{in}(1 - e^{-t/T}) \cong AE_{in}\ \frac{t}{T} \quad . \tag{41}$$

Thus viewed, a regenerative circuit may be considered as a non-regenerative circuit whose gain is greater than unity.

5. Wave Propagation and System Design

We have discussed the transient behavior of a switching circuit. Now we will go further into the transient behavior of a system. The sequence of transients of elementary switching circuits may be called "wave propagation" because any one transient in any one elementary circuit conveys one bit of information into succeeding stages.

Before discussing the propagation speed, we will introduce an important design parameter "stability factor."

5.1 Stability factor

In the viewpoint of switching speed, the circuit whose gain is less than unity is less problematical. It simply behaves as an attenuator with a delay time. The only thing we should do is to make the gain as close to unity as possible and the input to the circuit should be as large as possible.

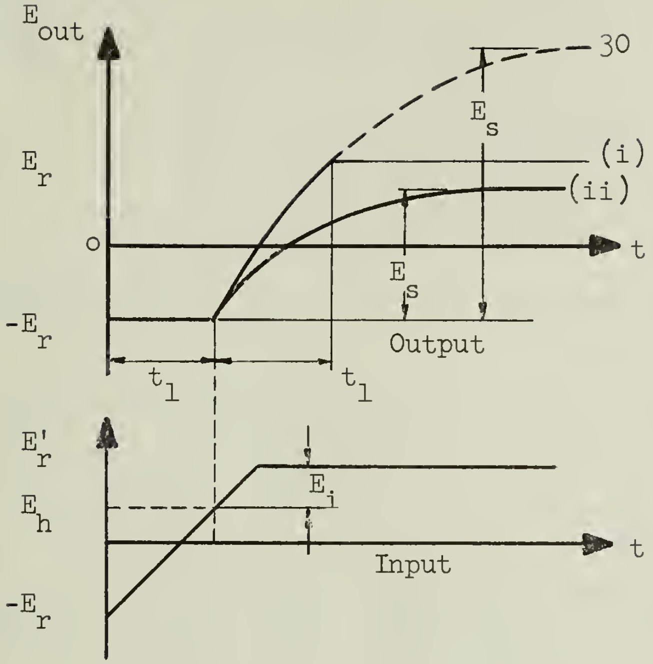


Figure 20: Input and Output

For the circuit, the gain of which is greater than unity, this is not all of the story. The transit time which is generally expressed by equation (34) is the function of $E_s/E_r = F$. As a matter of fact, F should be greater than unity. The greater F is, the smaller t_1 is. If F is sufficiently large, then the transition time will not be seriously affected by the variations of the circuit constants. Therefore F may be called the "stability factor." What is the minimum allowable magnitude of the stability factor? In order to answer this question, we will use the inverse gain-band-width k which is less subject to the variation of the circuit constants. For sufficiently large F, t_1 is

$$(t_1)_{min} = k\frac{E_r}{E_i} = \frac{kA}{F} \cong t_1 \quad . \qquad (42)$$

The variation Δt_1 of t_1 caused by the variation of A, which is also caused by the inevitable variation of circuit parameters, is

$$\frac{(\Delta t_1)}{(t_1)_{min}} = -\frac{1}{2F}\frac{\Delta A}{A} = -\frac{1}{2}\frac{E_r}{E_i}\frac{1}{A}\frac{\Delta A}{A} \quad . \qquad (43)$$

It is very desirable for logical designers of a system to make the $(\Delta t_1)/t_1$ small. To assure this to a logical designer, E_r/E_i, $1/A$, and $\Delta A/A$ must be kept satisfactorily small.

(i) $\frac{E_r}{E_i} \cdot \frac{1}{A} = \frac{1}{F}$ is related to

a) numbers of stages between wave shapers which will be explained in the following subsection; and consequently, the propagation speed of the system,

b) nominal values of available components.

(ii) $\frac{\Delta A}{A}$ is related to tolerances of available components.

The effort to find an economical compromise of both sides of equation (43) will finally specify the optimum (or minimum) stability factor. Since $1 - \alpha_o$ varies about 400% at most, $\Delta A/A$ may be greater than 100% under the current specifications. If $(\Delta t_1/(t_1)_{min}$ is desired to be, say, 10%, then F should be greater than 5.

Sometimes the "economical compromise" is an ambiguous solution and will not be further discussed. The corrected t_1 shown by equation (35) gives an optimum value for F to make t_1' minimum. Physically, this is not true, because the actual t_1 should always decrease as F increases. However it may be interpreted that the improvement owing to the increased stability factor will become very small when the stability factor exceeds a certain minimum value and that the optimum value obtained from equation (35) will give the minimum value. Thus obtained, the optimum value of F for ρ (in equation (35)) = 0.2, is 3. In the following discussions, the minimum value of the stability factor will be 3. If $(\Delta t_1/t_1)$ requires a value higher than 3, we may take it into consideration. However, in any case, it will be safer (more stable!) to design the system such that F is at least 3.

The critical deviation of the circuit parameters will now be defined as follows:

"When the deviations of the parameters cause $\frac{E_i}{E_r} A \leq (F)$ specified, then the parameters may be said to be 'critically deviated' with respect to the switching time." Notice that the term E_i/E_r contains the gains of the preceding stages and that this is a criterion to be applied to a system, not separate elementary circuits (this will be explained later).

This statement may be doubted because it does not contain any "time-dimension." This is all due to the fact that we have introduced the inverse gain-bandwidth which is a comparatively stable factor. If the required time determines a particular type of transistor, the average switching time is completely fixed. The worst switching time $(t_1)_{max}$ is

$$(t_1)_{max} = (t_1)_{av} \left[1 + \left(\frac{\Delta t_1}{t_{1_{av}}}\right)_{max}\right] \quad .$$

Therefore, to discuss $(t_1)_{max}$ (or $(t_1)_{critical}$) is to discuss $\left(\frac{\Delta t_1}{t_1}\right)_{max}$ which does not contain the time dimension.

5.2 Wave Propagation in a system

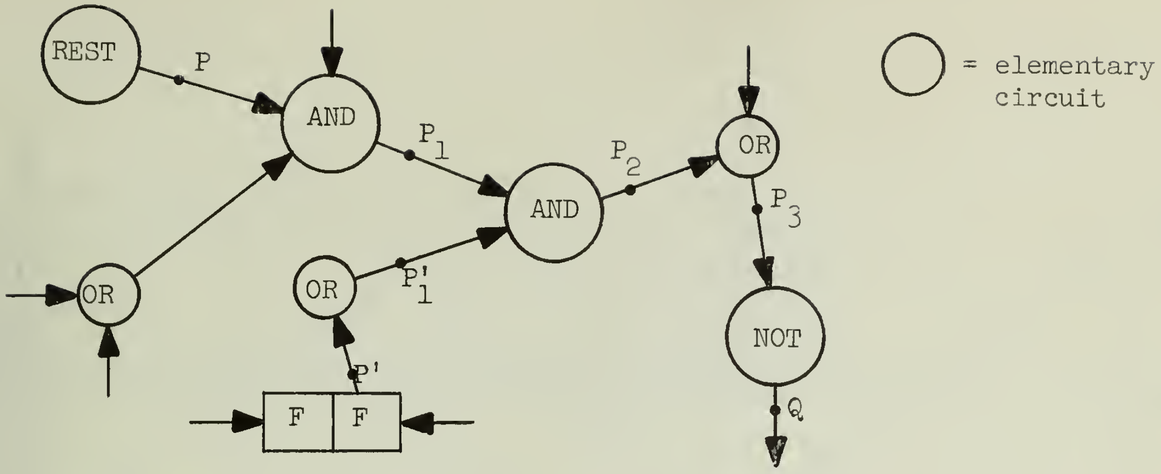
Let us consider a system in which waves originate at various points and propagate asynchronously. Is there any inherent wave propagation speed? Are the waveforms deformed after passing through many elementary circuits? Can not the waveform keep an inherent shape no matter how many circuits it passes through? Empirically, we know by observing the waveforms of an oscillating ring that there is an inherent waveform which is not affected by the length of the ring.

In preceding sections, the following things were concluded:

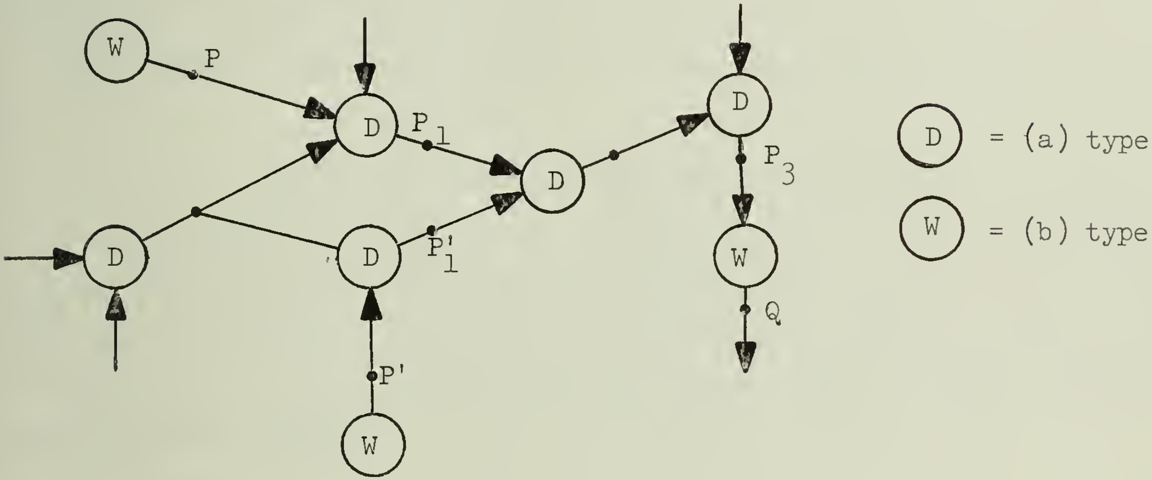
(i) In well-designed systems, there are two types of elementary circuits, i.e. a) $|A| < 1$, $T < t_o$, b) $|A| > 1$, $T > t_o$ where A is the gain, T is the time constant, and $2t_o$ is the transit time of the input waveform.

(ii) The a) type circuits act as a time delay unit with attenuation. The b) type circuits act as a wave shaper with certain time delay.

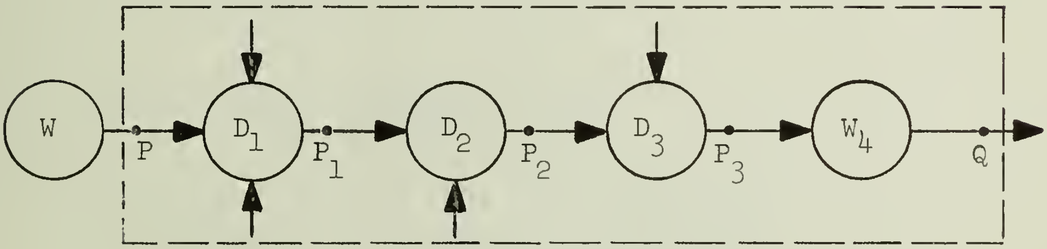
The emitter follower diode logic circuits will be classified as a) type (D). The collector follower, such as NOT circuits and flipflop circuits may be classified as b) type (W). Then, replacing the elementary circuits in the actual system (Figure 21(a)) by D or W, Figure 21(b) will be obtained. Now consider any path between adjacent W's, e.g., $P \longrightarrow P_1 \longrightarrow P_2 \longrightarrow P_3 \longrightarrow Q$ or $P' \longrightarrow P'_1 \longrightarrow P'_2 \longrightarrow P'_3 \longrightarrow Q$. The whole system is a complex of these paths, called a "unit chain," shown in Figure 21(c). Furthermore, each unit chain may be simplified into a unit box which consists of a certain delay and an ideal wave shaper. Propagation of a wave in a unit chain will be explained by Figure 22, which shows the worst possible case.



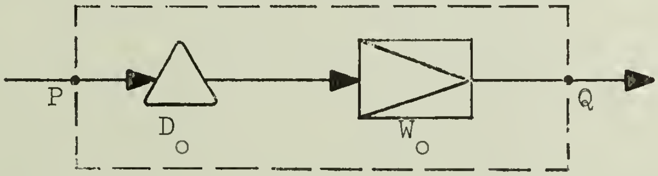
A. Actual system in which AND, OR are (a) type and FF, REST, NOT are (b) type



B. Simplified system in viewpoint of switching time



C. Unit chain



D. Unit box

Figure 21: Diagrammatic picture of system w.r.t. time

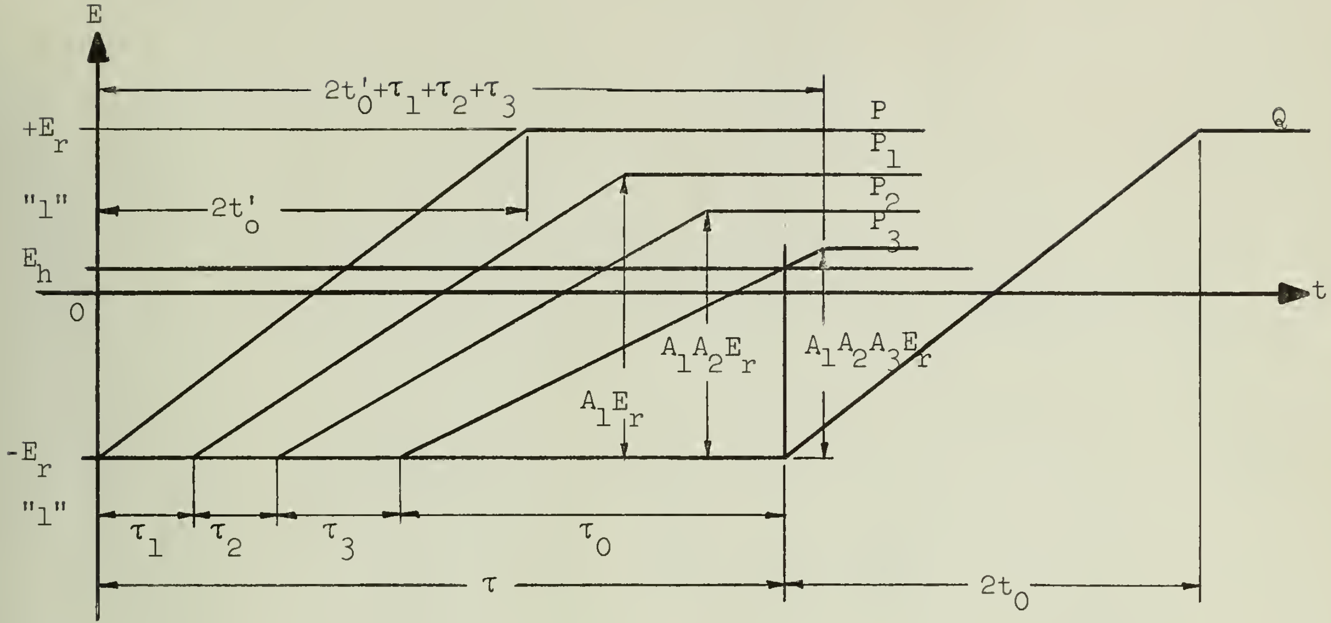


Figure 22: Wave Propagation in a Unit Chain

The actual elementary circuits have different types of delay times, such as the recovery time of diodes, and the delay of alpha. We will denote these delay times by d. Let T_i and A_i be the time constant and gain of the i^{th} delay unit in a unit chain, and T_0, A_0 be the time constant and gain of the associated wave shaper.

Then

$$\tau_i = T_i + d_i \qquad (44.a)$$

$$\tau_0 = \left(1 + \frac{1}{2D_T} + \frac{1}{2}\,\frac{E_h}{D_T E_r}\right) t_0' + d_0 \qquad (44.b)$$

$$t_0 = \frac{T_0}{A_0}\;\frac{1}{(2D_T - 1) - \frac{E_h}{E_r}} = \frac{k_0}{2D_T - 1 - \frac{E_h}{E_r}} \qquad (44.c)$$

where

$$D_T = A_1 \cdot A_2 \cdots A_n$$

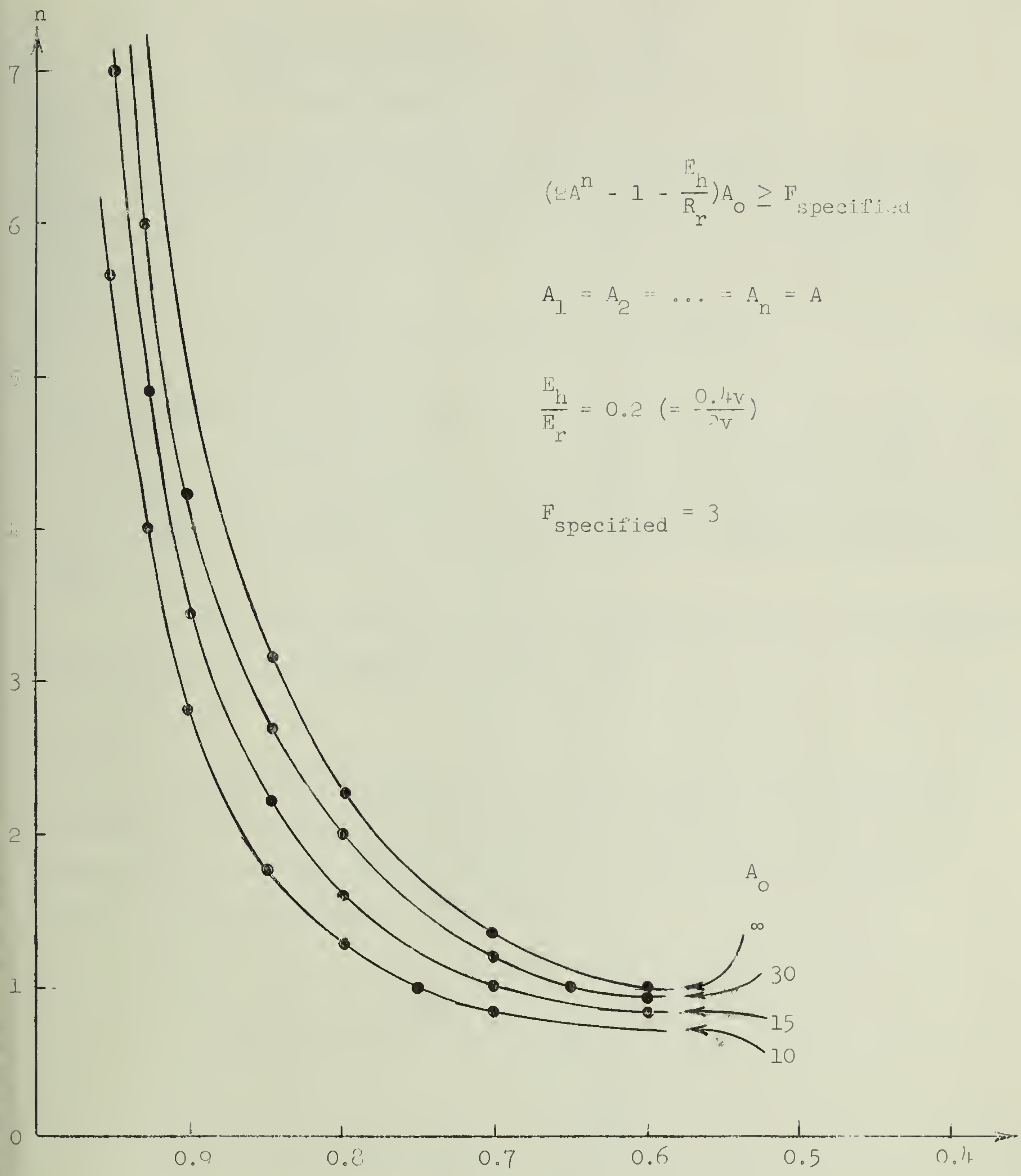


Figure Number of Delay Units in a Unit Chain

the total delay time τ of a unit chain is

$$\tau = \tau_1 + \tau_2 + \ldots + \tau_n + \tau_o , \qquad (44.d)$$

the output wave height is $+E_r$ or $-E_r$,

the transit time of the output wave is $2t_o$.

How many delay units can be held in a unit chain? The stability factor defined in section 5.1 will give the answer for this question. The total number of n in a unit chain must be such a number that equation (45) is satisfied.

$$\left(2 \cdot A_1 \cdot A_2 \cdots A_n - 1 - \frac{E_h}{E_r}\right) A_o \geq F \text{ specified} \qquad (45)$$

Figure 23 shows the allowable number n for a typical case. If the least gain of a delay unit is about 0.9 (=1 - 0.2v/2v), then the maximum allowable number is 5 for any case. If the gain of the wave shaper is finite, say 30, the number is 4. According to Figure 23, the gain of the delay unit has a more significant effect on n than that of the wave shaper.

If the wave shaper has nothing but restoring action, the propagation time t_p per bit may be defined by equation (46)

$$t_p = \frac{\tau}{n} \qquad (46)$$

Assuming that the delay units and wave shapers are constructed by the same kind of transistor, the inverse gain-band-width of which is k, the propagation time and the transit time will be rewritten in the following equation, (47), modifying the restriction (45):

$$t_p = k + d + \frac{1}{n}\,\frac{kA_o}{F}\left(1 + \frac{1 + \frac{E_n}{E_r}}{2A_1 A_2 \cdots A_n}\right) + \frac{d_o}{n} \qquad (47.a)$$

$$= k + d + \frac{1}{n}\,\frac{kA_o}{F}\; 1 + \frac{1 + \frac{E_n}{E_r}}{1 + \frac{E_n}{E_r} + \frac{F}{A_o}} + \frac{d_o}{n} \qquad (47.b)$$

$$t_o = \frac{kA_o}{F}$$

t_o/n is minimum for $A_o \cong \hat{A}_o$ (given by equation (47.c)) and the minimum walue is given by equation (47.d).

$$\hat{A}_o = \frac{2F}{\ln 2 - \frac{E_h}{E_r}} \tag{47.c}$$

$$\left(\frac{t_o}{n}\right)_{min} = \left(\ln \frac{1}{A}\right) \frac{4k}{(\ln 2)^2 - \left(\frac{E_h}{E_r}\right)^2} \tag{47.d}$$

Using the same magnitudes for parameters as those used in plotting Figure 23, and A = 0.97 for the average (not the least) gain of the unit delay, $\left(\frac{t_o}{n}\right)_{min}$ is about 0.25 k. The propagation speed is

$$t_p \cong k(1 + 0.5) + \left(1 + \frac{1}{n}\right) d \quad . \tag{47.e}$$

The propagation pattern shown in Figure 22 is a very primitive one. Taking this into consideration, the more probable average propagation time $\bar{t}_p$ may be

$$\bar{t}_p = \frac{n + 2}{n} k + \frac{n + 1}{n} d \quad . \tag{48}$$

Several different design philosophies of transistor-diode switching circuits have been reported. One of them is a "distributed gain" switching circuit.[11] This philosophy uses only wave shaper type circuits. The average propagation time designed by this philosophy will be (by Equation (37.a))

$$\bar{t}'_p = \frac{3}{2} k + d \quad . \tag{48}$$

The other one is a "concentrated gain" switching circuit. The so-called "emitter follower diode logic" circuit, which we are going to adopt, belongs to this class. If the allowable number n calculated by equation (45) for the worst case is greater than 4, then the "concentrated gain" circuit is faster than the "distributed gain" circuit. Furthermore, and this is a very important factor, the signal output impedance of the "gain larger than unity" circuit is always greater than that of the "gain smaller than unity" circuit. In sections 1 and 2, it was shown that the inverse gain-band-width linearly increases with the signal output impedance. This is an unfavorable factor for

the "distributed gain" circuits. For the new Illinois computer, the maximum allowable number n calculated by equation (45) may be 4~5. Therefore, the concentrated gain circuits may be justifiably applied.

At this point, the expected propagation speed of the new Illinois computer will be described. In the process of experimentation, it was observed that the delay time per emitter-follower was about 3 mμs. 2 mμs at most may be expected for diodes. k is about 4 mμs. Then from equation (48),

$$\bar{t}_p \cong 9 \text{ m}\mu\text{s}.$$

6. Dynamic Design Criteria - Conclusion

Given the elementary circuit configuration, the design will be carried on by considering the following things:

1. The transfer function of low level injection, small base width and non-saturating transistor switching circuits will be represented by equation (24):

$$G(s) = \frac{A}{1 + sT} \quad . \qquad (24)$$

2. The inverse gain-band-width k defined by T/A is a sort of inherent constant of the transistor. The k is directly and linearly related to the final speed of the system (5). Generally k will be expressed by equation (23):

$$k = K(1 + \omega_\alpha R_L C_c) \frac{\tau_\alpha}{d_o} \qquad (23)$$

where $K \cong 1$

R_L = equivalent load resistance

$\omega_\alpha = \frac{1}{\tau_\alpha}$ = alpha cutoff frequency

C_c = collector capacity

The chosen transistor will have a small C_c as well as a high ω_α. There is an optimum value of R_L to minimize k for a fixed required output voltage. This is due to the non-linearity of the transistor. The base driving impedance considerably increases k if $\omega_\alpha R_L C_c > 1$. Special care must be taken not to have a high output impedance.

3. Since (2) gives the conditions only for the magnitude of equivalent load resistance, all parameters must also satisfy the dc-logical requirements. In other words, (2) provides the conditions for the voltage swing to be required and (3) provides the conditions for the mean value of the voltage. The optimization criteria depend on the subjects designers are interested in. However, in any case, the "least expense" seems to be the only plausible criterion. To achieve this, we have to estimate the value of functions of the machine.

4. In order that the designed machine behaves stably, the stability factor F defined by $A \times E_{input}/E_{required} = F$ will be greater than a certain value. There is a minimum F for required stability ($\Delta t/t$), where t is the switching time. However in any case, F may be greater than 3.

5. There are two groups of switching circuits in a system. The one is the "gain less than unity" circuit and the other is the "gain larger than unity." The former, denoted D, acts like a delay unit with attenuation. The latter, denoted W, acts like a wave shaper with time delay. The system using both types may be called the "concentrated gain" circuit, while the system using only the latter will be called the "distributed gain" circuit. The number of D in a unit chain, which is a train of D's separated by two adjacent W's, is given by equation (45):

$$n = \frac{\ln \left(\dfrac{1 + \dfrac{E}{A_0} + \dfrac{E_h}{E_r}}{2} \right)}{\ln A} \tag{45}$$

where

A is the gain of D

A_0 is the gain of W

E_h is the threshold voltage of W.

If $n \geq 4$, then the propagation speed of the "concentrated gain" system is faster than that of the "distributed gain" system and given by equation (49):

$$\bar{t}_p = \frac{n+2}{n} k + \frac{n+1}{n} d \; [\, = (1 + 0.5)k + \frac{n+1}{n} d] \qquad (49)$$

If $n \leq 3$, then the "distributed gain" system will be faster unless the output impedance of the circuit is considerably higher, and the speed will be given by

$$\bar{t}_p = \frac{3}{2} k + d \quad .$$

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